Hardware Implementation of MIL-STD-1553 Protocol Over OFDMA-PHY Based Wireless High Data Rate Avionics Systems

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***Abstract*—In this paper, a method of improving data rate in avionics systems is proposed which incorporates OFDM transmission technology for high data rate communication. An FPGA-based hardware test bed is developed which uses OFDM physical layer over MIL-STD-1553B communication in RF wireless systems. Finally, a prototype test system is developed using three nodes to emulate Wireless Avionics Intra-Communications (WAIC) over RF systems. The implementation is done on Wireless Open-Access Research Platform (WARP). WARP has virtex-4 FPGA in its core for processing and radio daughter cards that can perform over the air data transmission and reception over 2.4 GHz and 4.5 GHz bands. The real-time performance of the proposed and implemented system is tested using over the air transmission and reception of data traffic. The result shows significant improvement of over the air throughput improvement as compared to the traditional avionics systems with an average Bit Error Rate (BER) satisfying 10^{-3}.**

Keywords: MIL-STD-1553B, OFDMA, FPGA, Hardware Implementation, Avionics, Test Bed, Wireless Avionics Intra-Communications, High Data Rate.

I. Introduction

Over the past few decades, MIL-STD-1553 has been one of the most promising candidates for communication over avionics systems. It has found its use in a wide range of military applications such as aircraft control, missile, ships, tanks and satellite communications. The reason for its wide acceptability is the error detection capability, high reliability, noise immunity and deterministic behavior. MIL-STD-1553 is a standard Time Division Duplexing (TDD) based bi-directional communication protocol that relies on transmission and reception of data through command-response method providing a data transfer rate of 1 Mbps over the avionics bus. In a Traditional avionics bus, employing MIL-STD-1553 protocol consists of three major terminals, namely Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) having a total of maximum 32 terminals.

There has been considerable research to increase the speed of legacy MIL-STD-1553 systems [1], [2]. Many solutions have been proposed which efficiently increase the transmission speed of avionics buses such as Fiber Distributed Data Interface (FDDI), Fire Wire (IEEE 1394) and Fast Ethernet (FE). These solutions have replaced the legacy aviation bus to a modified high-speed data bus. In [3] and [4], studies have been proposed to replace the legacy wired MIL-STD-1553 bus by a high-speed Optical Wireless Links (OWL) for use in Intra Satellite Communication (ISC). In [5], compatibility of broadband Orthogonal Frequency Division Multiplexing (OFDM) based radio frequency (RF) link interface to aviation bus is presented.

OFDM is the most extensively used physical layer radio access technology in modern wireless systems because of its better bandwidth utilization, high reliability, simpler channel equalization and relatively easy implementation using FFT to generate orthogonal subcarriers [6]. A typical OFDM system with 5 MHz bandwidth can easily achieve 20 Mbps in SISO configuration

Over the past few years, the avionics communication system has experienced a massive expansion of interconnected subsystems and data exchange rate thereby increasing complexity on interconnect. In modern aircraft, the communication cabling weighs nearly as 2-5% of the aircraft's weight, and cabling length goes nearly up to 280 miles [7]. Thus Wireless Avionics Intra-Communications (WAIC) has emerged as the most promising candidate for communication for the intra-aircraft avionics communication system. Application of WAIC on aircraft is often termed as Fly-by Wireless. WAIC can reduce nearly 30-40% of total cabling required in aircraft thereby reducing the aircraft weight and hence increasing the fuel efficiency. The recent trend of study over the last few years focuses on the possible challenges and finding suitable solutions for WAIC communications. In [7], opportunities and challenges on WAIC over RF and its potential PHY-MAC solutions are discussed. In [8] and [9], channel characterization of WAIC system is reported for 5 GHz and 4.2-4.4 GHz band respectively. In [10], suitability of WAIC over 4200-4400 MHz band is discussed by taking into consideration the effect of interference of WAIC system to radio altimeter. Till date, this band has emerged as the most promising band for WAIC communications. A real-time test bed for high data rate WAIC is considered essential to achieve a proof of concept and establish suitability of such a system for avionics applications. To the best of knowledge of the authors, such a test bed is not yet been reported in literature.

The objective of this work is to develop RF based avionics test bed system with high data rate by incorporating OFDM as the physical layer transmission technology. The MIL-STD-1553 communication protocol is implemented for communication over wireless avionics busses. The test bed

system is extended to realize a WAIC system. The real-time measurements provide proof of concept that is very helpful while building full scale systems.

II. System Model

The objective of this work is to replace the power hungry and heavy traditional MIL-1553 bus by a wireless bus based on RF links. As discussed in section I, this can be obtained by employing OFDM based RF links. Fig 1 provides the overall system architecture of the system that is to be designed. There are three kind of nodes in the bus, namely BC, RT and BM. The hardware design of all the three types of nodes is same only for the functionalities which differ based on the data link layer of the nodes. Each node consists of one pair of transmitting and receiving antennas for transmission and reception of RF signal respectively. The Radio Front End (RFE) of each node enables the down conversion of the signal to baseband level and gain adjustment in transmitter, receiver as well.

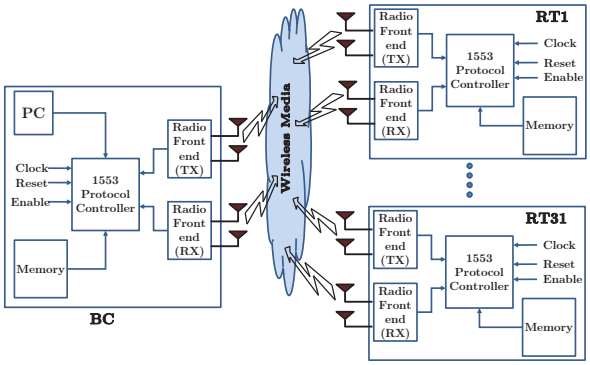


Fig. 1: Overall System Architecture

Fig 2 depicts the baseband processing system that is essentially an OFDM PHY system. At the transmitter, the packets are formed by adding 32 bit Cyclic Redundancy Check (CRC) code corresponding to each OFDM symbol. The data packets pass through convolution encoder for Forward Error Correction (FEC). The choice of the code rate is flexible, and a code rate of 1 implies that no FEC encoding at the transmitter. The Symbol Mapper maps incoming data into constellations. IFFT does the generation of orthogonal subcarriers and multiplexing. Route to Antennas and TX Processing routes the signal to different antennas and resamples the data using the proper sampling rate respectively. Finally, RF front end consists of upconverter, DAC and Variable Gain Amplifier (VGA) and antenna for send and receive of RF signal.

At the receiver side, In the RF front end, the received RF signal is downconverted, gain adjusted in VGA and passed through Analog to Digital Converter (ADC) to get the digital baseband signal. Synchronization, Packet Detection and Carrier Frequency Estimation (CFO) estimation and correction is performed at MIMO-SYNC block. The signals are collected and re-sampled to the processing frequency in Collect From Antennas (CFA) and Rate Matching block

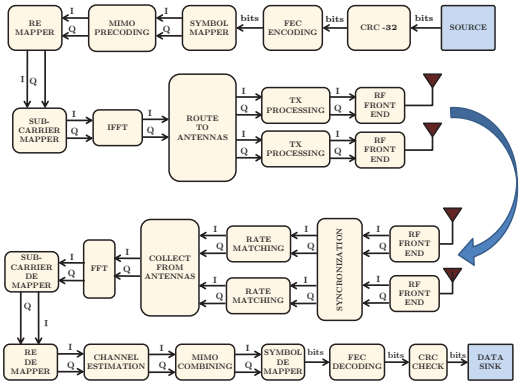


Fig. 2: Physical Layer System Model

respectively. Generation of orthogonal subcarriers and demultiplexing are accomplished in FFT. Channel estimation in pilot subcarriers followed by a time-frequency interpolation produces the estimated channel coefficients over the entire transmission bandwidth using which channel equalization is performed. The equalized signals are demodulated at symbol de-mapper to produce bits from constellations. Forward error correction is performed using Viterbi decoding followed by CRC detection to check for packet error.

OFDM symbols carry a large number of bits. In fourth generation (4G) systems, which use Orthogonal Frequency Division Multiple Access (OFDMA), one sends multiple symbols over a single Transmit Time Interval (TTI). This concept is applied in this work to design a frame structure that resembles the traditional MIL-STD-1553 packet format. Fig 3 depicts the packet format used in this work. One TTI corresponds to 12 OFDM symbols out of which the first two OFDM symbols are reserved for synchronization, packet detection, CFO estimation and correction. The Rest of the 10 OFDM symbols are granted for data transmission. Each of them is used to form either a data word or command word or status word. Fig 4 provides the frame structure of command word and data word in the time-frequency domain. OFDM symbol used for command word or data word are uniquely determined by two 24 bit unique orthogonal pseudo-random sequences. The transmission protocol remains unaltered and the duration of any communication viz. BC to RT, RT to BC and RT to RT is restricted to one subframe time i.e. one millisecond. This leads to a maximum of 9 data word for BC to RT communication and 10 data word for RT to BC and RT to RT communication.

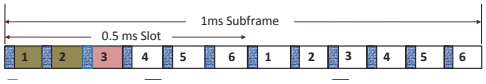


Fig. 3: Time Domain Packet Format

The system successfully provides a demonstration of all three types of communication. The advantage of the wireless bus makes the prototype test bed mobile. The development of the prototype test bed and the collection of test bed results

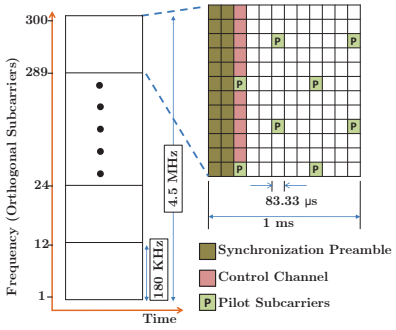


Fig. 4: Frequency Domain Packet Format

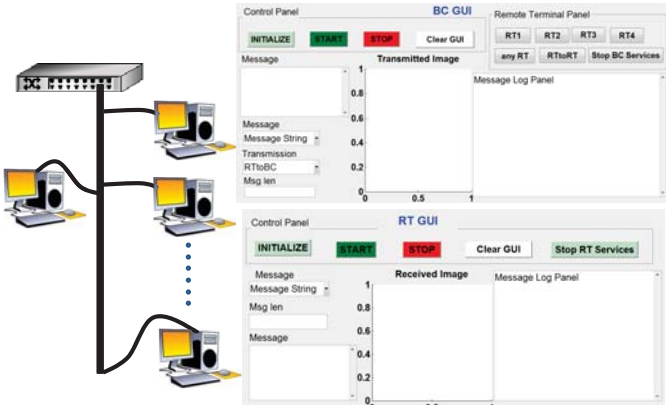


Fig. 5: Simulation Based Framework over TCP/IP

have been made under certain parameters and assumptions. These are as follows.

1) RT is assumed to be a simple version of RF transceiver that does not include any Automatic Gain Control (AGC) in it. BC controls the transmitter gain according to the distance of separation between BC and RT.
2) The performance of this system is measured without employing FEC at the receiver. The system considers a BER threshold of 10^{-2} for determining the packet to be in error.
3) The system employs WLAN preamble based synchronization. This produces timing offset in the received signal. However, the over the air performance measurement is done under perfect frame synchronization.

III. Hardware Test Bed Implementation overview

The development of the hardware test bed has gone through different phases. First a simulation-based framework is implemented using TCP/IP over Ethernet LAN. In this phase, the work described in [11] is reproduced. In the next phase, the framework is extended for use in TCP/IP over Wireless LAN (WLAN). Finally, the custom OFDM PHY and MAC layer is implemented to develop the hardware test bed. Following are the detailed description of both simulation and hardware test bed.

A. Simulation Framework for MIL-STD-1553

Fig 5 shows the overview of the simulation-based framework that is implemented in the initial phase. BC and RT's are realized using PC having a configuration of quad core CPU of 2.5 GHz processing frequency. Ethernet based Local Area Network (LAN) is used to realize the common bus. The MIL-STD-1553 protocol is realized in MATLAB. A Graphical User Interface (GUI) is developed for user interaction, external control and transmit/receive data traffic. The framework is extended to communicate over wi-fi based WLAN. The protocol and overall implementation remains same.

B. Hardware Test Bed for MIL-STD-1553 over custom OFDM PHY

The functionality of the physical layer is already described in section II. All the physical layer algorithms are implemented in a single Xilinx Virtex4 FPGA chip. The FPGA contains a Power PC (PPC) microcontroller for the use of Physical layer control and to develop driver and API for interfacing external components. Fig 6 illustrates the detailed hardware architecture of each node in the testbed design. Each nodes consists of custom OFDM transmitter(OFDM Tx) and receiver (OFDM Rx) chains implemented in FPGA. PPC controls the parameters of PHY using 256 Kb of shared memory configured in the FPGA. Data handshake between the application interface and PPC is achieved via Ethernet interface using the API's written in PPC core. A debug interface is developed using serial communication. Radio cards embedded on the board are used to transmit and receive RF signals over the air. The baseband signals before upconversion are passed to analog cards embedded on the board and viewed in Digital Storage Oscilloscope (DSO) for real-time monitoring of signals.

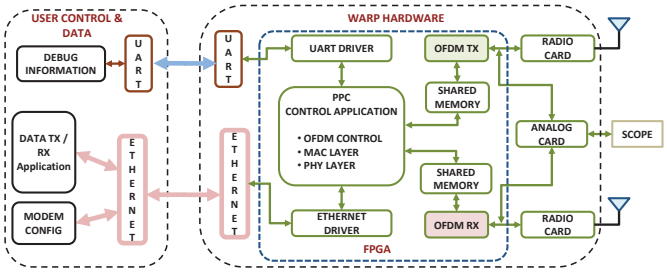
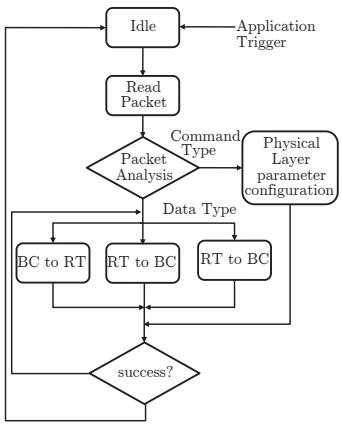


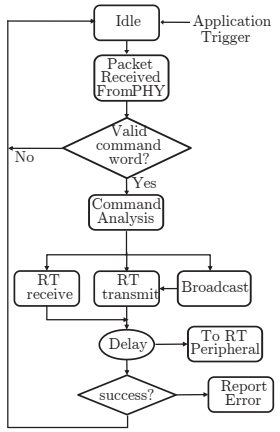
Fig. 6: Detailed Hardware Architecture of Hardware Test Bed

Fig 7a illustrates the state machine diagram for MIL-STD-1553 MAC implementation at BC side. In the BC-MAC module, the state machine starts to run at the external trigger from the application. The user application can send two type of packets upon the external trigger. The first type of packets is referred as command type packets which are used to configure the physical layer parameters such as modulation type, antenna configuration, gain control, RF channel selection and physical layer status detection. The second type of packets, referred as data type packets are used to initiate the communication in the bus. Upon the reception of packets from the application, the packets are analyzed, and the particular job is executed. In all,

four types of jobs are executed in this level, namely BC to RT communication, RT to RT communication, and physical layer parameter configuration. Upon the successful completion of the job, it again returns to the idle state and waits for initiation of next communication.



(a) State Machine Diagram of BC Module



(b) State Machine Diagram of RT Module

The RT-MAC module controls the working process of RT. Fig 7b explains the state machine diagram of RT-MAC module. The MAC layer process is triggered by the valid reception of a packet from the physical layer. Upon reception of a valid packet, the first OFDM symbol is extracted to receive the command word. The RT checks the command word to know if he is the intended recipient. If the command word is a valid receive command word, RT receives the next incoming OFDM symbols as data words. After successful reception of data words, RT sends an OFDM symbol containing a status word. At BC, the successful completion of BC to RT communication is recognized by analyzing the status word from RT. If the command word is a valid transmit command, the RT sends a subframe in which the first OFDM symbol is the status word and the rest are data words. In the BC side, upon the successful reception of status word, the data words are extracted from the next OFDM symbol in the subframe.

In RT to RT communication mode, the BC sends two OFDM symbols in a TTI, First one containing receive command for receive RT and the second one contains a transmit command for the transmitter RT. Upon the reception of a valid transmit command, the transmit RT sends a subframe containing status word followed by data words. Upon the reception of a valid receive command in receive RT, it waits in the receiver mode and receives the data words sent from the transmitting RT. At BC, the successful completion of the process is recognized by sequentially receiving and analyzing status word from transmitting RT and receiving RT respectively.

IV. FPGA Design Platform

The WARP hardware [12] provides a platform for implementing and testing physical layer algorithm in real time as it is equipped with a Virtex-4 FX100-11FFG1517C FPGA having 42K logic slices, 160 Xilinx DSP-48 blocks and four radio cards that are capable of operating at 2.4 GHz and 4.5 GHz frequency with a bandwidth of 40 MHz. It also provides the facility of varying transmitter-receiver gains that are very helpful while testing the performance of any algorithm in real time.

A. Testbed Design Flow

Fig. 8 shows detailed design flow for the hardware implementation of the test bed. The design undergoes several phases of implementation.

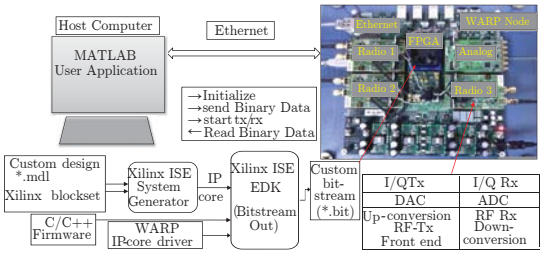


Fig. 8: Design Flow in WARP

- Physical layer processing is implemented in FPGA processing unit using the system generator tool provided by Xilinx. It uses Simulink workspace for the development environment, Xilinx library blocks are used for the RTL logic design. Finally, an IP core is generated upon successful compilation of the design.
- The system generator IP-core is imported to Xilinx Embedded Development Kit (EDK) tool. Here the IP core generated in system generator is interfaced with other hardware specific driver IP-cores
- A firmware program is written into PPC that controls the physical layer module. This program is written in C++.
- A user application is written in MATLAB that sends and receives data traffic to/from the hardware through ethernet interface.

V. Experimental Test System

Fig 9 presents the experimental test setup developed for the demonstration of MIL-STD-1553 over OFDM. A module consists of a WARP node connected to PC via ethernet that can be configured either as BC or RT. The setup consists of three modules, one configured as BC and the other two configured as RT's. Both BC and RT feature GUI for transmission and reception of data traffic and configuration of modules.

VI. Implementation Results

A. Hardware Resource Usage

Table I provides the post-synthesis results of resource utilized in hardware. From the synthesis results, it is clear that the design of this type of system can be implemented in a single virtex4 FPGA core with an average resource utilization of nearly 60%. The area efficiency can be made to increase further by efficient distribution of memory and logic resource elements over the design. Furthermore, the design is made

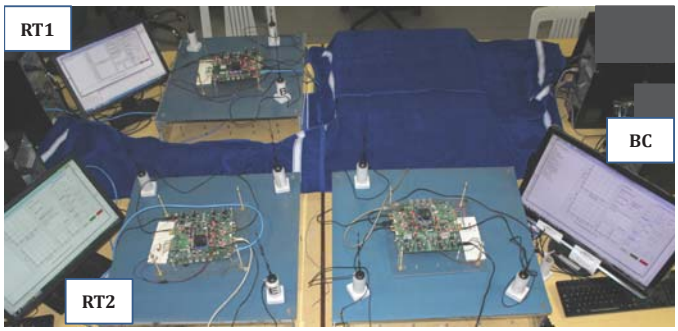


Fig. 9: Experimental Set Up

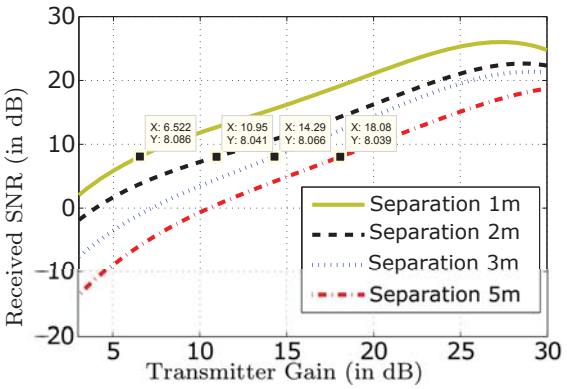


Fig. 10: Received SNR vs Transmitter Gain for Various Distance

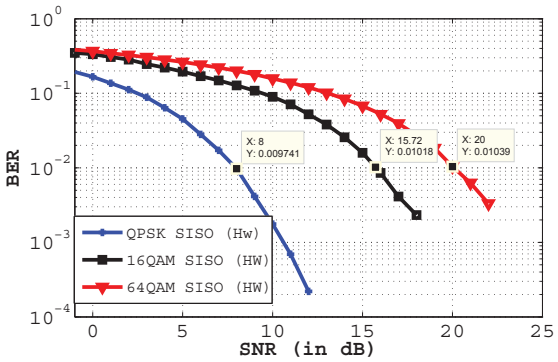


Fig. 11: BER vs SNR Performance for SISO Configuration

flexible to work with different configurations with minimum physical layer design alteration possible. Consequently, the memory and logic resource usage has increased a bit.

Table II provides the power consumed by the design in the hardware. The power consumption result is obtained using Xilinx's Xpower tool. Even though there is no optimization performed for power efficiency of the design, from the synthesis results it is clear that the design does not consume a significant amount of power while running the PHY-MAC design.

TABLE I: FPGA Resource Usage

Resource Type	Total Available	Usage	Percentage Usage
Slice	42176	19360	46%
LUT	84352	54887	65%
BRAM	376	274	72%
DSP 48	160	86	53%

TABLE II: Power Consumption in FPGA

Type	Power Consumed (mW)
Logic Power	134
Signalling Power	108
Total Power	242

B. Performance Evaluation Results

Finally, the performance of this designed OFDMA PHY based avionics test bed is evaluated by using real time over the air transmission and reception of data traffic through the designed test bed. Next, over the air results are collected and analyzed in the MATLAB workspace. The performance evaluation is done through the following phases.

1) PHY Layer Performance Evaluation Results: The performance of PHY layer algorithms is tested at various Signal to Noise Ratio (SNR) values. The PHY layer transmit-receive gains and distance plays an important role in the received SNR in the receiver. Fig 10 illustrates the variation of SNR with the transmit power and distance. In this procedure, the receiver gain at the receiver is kept at a constant value.

Fig 11 illustrates the Bit Error Rate (BER) performance at various SNR conditions. This BER performance evaluation is done for uncoded systems. Using the two results as mentioned above, a suitable value for transmit gain is chosen depending on the transmitter and receiver separation. This process is done by taking a BER threshold of $10^{-}2$ and finding the corresponding SNR values on the BER performance curve. Next, a suitable transmit gain depending on the distance is found from the SNR results mentioned in Fig 11.

Fig. 12 illustrates the Data Rate vs. SNR performance for various modulation schemes. The data rate shown here is essentially an application layer throughput obtained by setting packet BER threshold of 10^{-2} for packet error. From the results, a maximum of 1.5 Mbps is achievable at the application layer. This is so because the data transfer speed at the application and WARP PHY-MAC node interface limits the throughput achievable at the application layer throughput. Table III shows the over the air throughput obtained at 22 dB for various modulation schemes which is much higher. Clearly, a high-speed application to PHY interface can significantly improve the overall system throughput.

TABLE III: Over the Air Throughput for Various Modulation Schemes

Modulation	Over The Air Throughput (Mbps)
QPSK	5.598
16QAM	11.18
64QAM	16.54

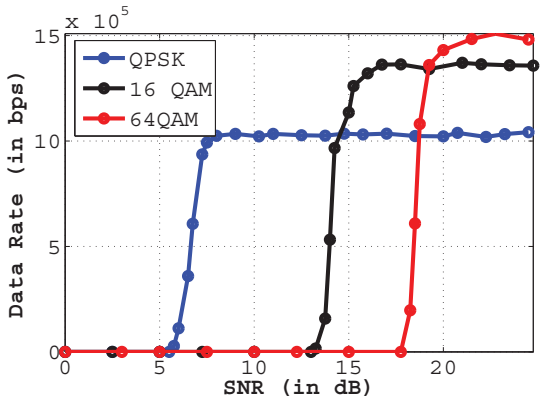


Fig. 12: Data Rate vs SNR Performance for Various Modulation Schemes

2) MAC Layer Algorithm Performance Evaluation Results: Fig 13 demonstrates Packet Error Rate (PER) performance for various modulation schemes at a two-meter distance of separation between BC and RT. Fig 13 depicts the statistics of the received packets for an over the air transmission and reception of 1000 packets through the test bed. From the PER performance, it is found that a PER performance (Fig 13) of 10^{-2} is achievable with a transmitter gain of 12 dB at BC. This result carries significant importance as RT does not employ any AGC and hence BC controls transmitter gains to achieve a satisfied PER performance.

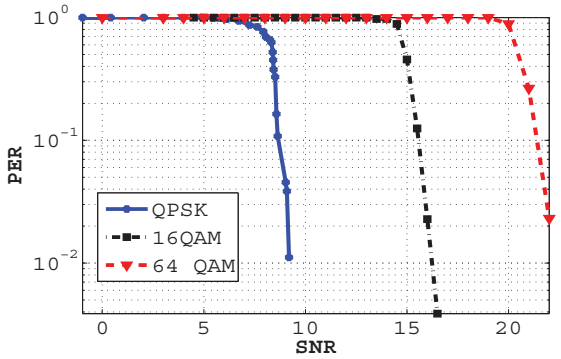


Fig. 13: Packet Error Rate vs SNR for Various Modulation Schemes

VII. Conclusion

In this paper, a method of improving the throughput of avionics system using OFDM as PHY layer transmission technology is discussed. An FPGA-based test bed is developed which uses the MIL-STD-1553 protocol based communication over OFDM physical layer. The design is implemented in WARP hardware, an FPGA-based embedded system capable of RF communication. The implementation result shows that the transceiver node can be realized inside a single FPGA with overall 60% of overall area utilization and low power requirements. The system is made flexible to work with different configurations with minimum physical layer design alteration possible due to which the designed system has relatively high memory requirement. A WAIC test system is designed using three WARP nodes one configured as BC and other two configured as RT. Real-time over the air performance results are obtained using data transmission at 2.4 GHz band through the test system. This work assumes that RT has simple RF front end and does not employ any AGC, and hence the optimum transmitter gain at BC for the various distance of separation between BC and RT is found. This result carries significant impact on the overall performance of the system. It is shown that the over the air throughput of the system can reach up to 16.54 Mbps at 22 dB of SNR using SISO configuration for 5 MHz of transmission bandwidth. This result clearly shows a significant improvement in throughput over traditional avionics systems throughput of 1 Mbps. However, The data transmission is also achieved at 4.5 GHz band.

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